



H-706-02

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

K. ITOH et al.

Serial No. 09/864,338

Group Art Unit: 2818

Filed: May 25, 2001

Examiner: S. Mai

For: LARGE SCALE INTEGRATED CIRCUIT WITH
SENSE AMPLIFIER CIRCUITS FOR LOW VOLTAGE OPERATION

INFORMATION DISCLOSURE STATEMENT (IDS)
UNDER § 1.97 AND § 1.98

Commissioner for Patents
Washington, D.C. 20231

Sir:

1. This IDS should be considered:

(a) when filed within three months of the filing date of the present application, or within three months of the filing date of the National Stage as set forth in § 1.491 in an international application, or before the mailing date of a first Office Action on the merits, whichever occurs last;

(b) when filed before the mailing date of either a Final Rejection under § 1.113 or a Notice of Allowance under § 1.311, whichever occurs first and when 1(a) does not apply. For this purpose, there is included herein either a certification in section 4 below (included when indicated by a marked box), or a fee of \$180.00 (a check in the amount of \$180.00 is enclosed, or if not see section 5 below);

(c) when filed prior to the payment of the Issue Fee, when 1(a)-(b) do not apply, and when a certification is included in section 4 below (included when indicated by a marked box); then the Applicant(s) hereby petition(s) and request(s) consideration of this IDS, and provided herewith is a fee of \$180.00 (a check in the amount of \$180.00 to cover the petition fee, or if not see section 5 below).

Handwritten signature and date 11/24/02

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2. When 1(a)-(c) do not apply, then it is requested that this IDS be placed in the file.

3. Listing of the information submitted is on the attached Form PTO-1449, which forms a part of this IDS. A copy of each listed document is enclosed when needed (needed for U.S. and foreign patents, publication or portion thereof listed; no copy of a U.S. patent application is needed; a copy of a document is not needed when previously submitted or previously cited by the PTO in a parent application of the present application as set forth under 35 U.S.C. § 120).

4. Submitted herewith are English translations of the following two cited references by a JPO Office Action of March 27, 2001 against counterpart JP Appl. No. 10-369011. Please note that these two references are already listed in the IDS of July 12, 2001.

58-211391

63-229848

Also enclosed are the following three new references with the attached English abstract:

54-137246

61-160975

60-48525

Additionally, the following abstract, which forms a statement of relevance, is provided for Japanese Application No. 60-48525.

The reference discusses that "in order to increase integration density, a technique of scale-down of devices (i.e. shrinking the channel length) has a problem that power consumption decrement is difficult because of degradation of current OFF characteristics and increase of leakage current of channel of transistors" in the section [PRIOR ART]. Then, the reference mentions that "a purpose of this invention is to eliminate the above mentioned problem and provide a CMOS type microcomputer which suppresses leakage current at a stand-by state and is able to be low power consumption" in the section [PURPOSE OF THE INVENTION]. The constitution of the

invention is understood by the foregoing Abstract and Fig. 2 of the reference.

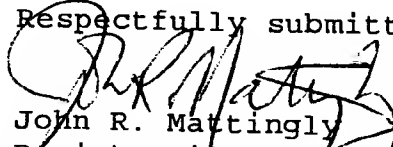
Also, an English language Abstract, which forms a statement of relevance, is submitted for JP61-24090 (English translation of the text is enclosed), JP57-142032 and JP54-72691. For JP54-72691, U.S. Patent No. 4,233,672 is an equivalent, copy enclosed.

5. If a fee or additional fee is required, the Commissioner is hereby authorized to charge any fee or additional fee that may be required and credit any excess to Deposit Account No. 50-1417. A duplicate of this sheet is attached.

6. No explanation of relevancy is being provided for the following document(s) because each is either in the English language, discussed in the present Specification, or its relevance is as stated in a communication from a foreign patent office in a counterpart foreign application, copy enclosed.

7. If the PTO determines that part(s) of the required content is inadvertently omitted, then it is requested that the Applicant(s) be given additional time and specific identification of such omission(s) to enable full compliance.

Respectfully submitted,


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